SGS-THOMSON MICROELECTRONICS

QUALITY & RELIABILITY REPORT

April 1994 to March 1995 - EPROM, FLASH MEMORY, EEPROM and SRAM Products

INTRODUCTION

SGS-THOMSON manufactures a wide range of memory types which include:

Non-volatile memories: FLASH Memory, EPROM, OTP ROM and EEPROMs. EPROM products are manufactured in both 1.5µ NMOS and 0.8 to 0.6µ CMOS technology; FLASH Memories in 1.2 to 0.6µ CMOS technology; OTP ROMs in 0.8 to 0.6µ and EEPROMs in 1.5 to 1.0µ CMOS technology.

Packages for non-volatile memories include both ceramic FDIP and plastic PDIP, PLCC, SO and TSOP.

Static RAMs: Fast SRAM, both Synchronous and Asynchronous and NVRAMs (ZEROPOWER and TIMEKEEPER ranges). Fast SRAMs are manufactured in 0.7-0.6µ HCMOS technology; NVRAMs in 1.2-0.8µ HCMOS.

Packages for Static RAM products include the plastic PDIP, PLCC and SOJ. Some of the ZEROPOWER and TIMEKEEPER products use a modified PDIP 0r SO with an additional "top hat" assembly mounted above and containing a Lithium battery and optionally a quartz crystal. The battery and crystal are sealed in the plastic cap with a plastic resin.

The results presented in this quarterly report cover the tests made from April 1994 to March 1995. Regular reports are issued each quarter with the last years cumulative results.

Director of
Memory Products Group
Quality Control & Reliability

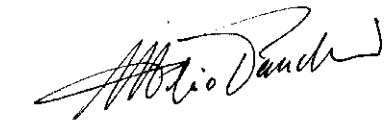

Table 1. NMOS E3/1.5µm Process UV EPROM Reliability Data, Die Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M2716		M2732A		M2764A		M27128A		M27256		M27512	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,												
		– 48 hrs	190	0	158	0	15,174	0	6,527	0	13,486	0	3,655	0
		– 168 hrs	190	0	158	0	1,617	0	1,521	0	1,151	0	2,340	0
		– 500 hrs	190	0	158	0	785	0	351	0	1,151	0	351	0
		– 1000 hrs	190	0	158	0	785	0	351	0	1,151	0	234	0
Retention Bake	1008	250°C,												
		– 48 hrs	170	0	200	0	900	0	500	0	500	0	900	0
		– 168 hrs	170	0	200	0	900	0	500	0	500	0	900	0
		– 500 hrs	170	0	200	0	900	0	500	0	500	0	900	0

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 2. CMOS E5/0.8µm Process UV EPROM Reliability Data, Die Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C64A	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,		
		– 48 hrs	2,964	0
		– 168 hrs	500	0
		– 500 hrs	500	0
		– 1000 hrs	400	0
		– 2000 hrs	-	-
Retention Bake	1008	250°C,		
		– 48 hrs	200	0
		– 168 hrs	200	0
		– 500 hrs	200	0

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 3. CMOS E5/0.8µm Process (–10% upgrade) UV EPROM Reliability Data, Die Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256B (B) M87C257	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz, (50% '0')		
		– 48 hrs	24,963	0
		– 168 hrs	400	0
		– 500 hrs	400	0
		– 1000 hrs	400	0
		– 2000 hrs	-	-
Retention Bake	1008	250°C, (99% '0')		
		– 48 hrs	300	0
		– 168 hrs	300	0
		– 500 hrs	300	0

Table 4. CMOS E5/0.8µm Process (-20% upgrade) UV EPROM Reliability Data, Die Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C512 (C)		M27C1001 (C)		M27C1024 (B)		M27C2001 (C)		M27C4001 (D)		M27C4002 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,												
		– 48 hrs	12,134	0	15,715	0	4,743	0	5,821	0	4,867	0	9,705	0
		– 168 hrs	1,200	0	2,702	1 (a)	200	0	200	0	1,248	0	80	0
		– 500 hrs	1,200	0	1,353	0	200	0	200	0	576	0	80	0
		– 1000 hrs	1,200	0	1,176	0	200	0	200	0	480	0	80	0
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	250°C,												
		– 48 hrs	700	0	1,456	0	100	0	60	0	600	0	100	0
		– 168 hrs	700	0	1,456	0	100	0	60	0	600	0	100	0
		– 500 hrs	700	0	1,256	0	100	0	60	0	600	0	100	0
		– 1000 hrs	-	-	60	0	-	-	-	-	-	-	-	-
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-

Note: a. Contact spiking (barrier defectivity)

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 5. CMOS E5/0.8µm Process (-35% upgrade) UV EPROM Reliability Data, Die Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (E)		M27C2001 (E)		M27C4001 (E)		M27C801		M27C160	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,										
		– 48 hrs	4,209	0	2,190	0	11,149	0	2,159	0	1,904	0
		– 168 hrs	1,056	0	225	0	1,894	0	218	0	283	0
		– 500 hrs	96	0	225	0	1,024	0	218	0	283	0
		– 1000 hrs	96	0	225	0	832	0	218	0	283	0
		– 2000 hrs	96	0	144	0	550	0	-	-	-	-
Retention Bake	1008	250°C,										
		– 48 hrs	400	0	150	0	1,096	0	283	0	293	0
		– 168 hrs	400	0	150	0	1,096	0	283	0	293	0
		– 500 hrs	300	0	150	0	996	0	283	0	293	0
		– 1000 hrs	100	0	100	0	546	0	233	0	243	0

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 6. UV EPROM Reliability Data, Package Related Tests (Ceramic Frit-Seal), April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	Samp.	Fail
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 3,300 3,300 1,250	 0 0 0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Thermal Shock	1011	–55 to 125°C, – 60 cycles	 175	 0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Salt Atmosphere	1009	Test Condition A, 35°C	25	0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Solderability	2003	245°C, 5sec, Precondition Steam, 1hr	935	0
Resistance to Solvents	2015	4 Solvent Solutions	244	0
Lead Integrity	2004	Test Condition B2 (lead fatigue)	75	0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		

Test Procedure	MIL-STD-883 Procedure	Test Conditions	Samp.	Fail
Environmental Sequence:				
1. Thermal Shock	1011	–55 to 125°C, 15 cycles		
2. Temperature Cycling	1010	–65 to 150°C, 100 cycles	50	0
3. Moisture Resistance	1004	–10 to 65°C, RH = 90%, 10 cycles of 24hrs		
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Mechanical Sequence:				
1. Mechanical Shock	2002	Test Condition B		
2. Vibration Variable Frequency	2007	Test Condition A	75	0
3. Constant Acceleration	2001	Test Condition E		
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Temperature Cycling	1010	–65 to 150°C, 10 cycles		
Constant Acceleration	2001	Test Condition E	80	0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		

Table 7. CMOS E5/0.8µm Process (–10% Upgrade) OTP ROM Reliability Data, Die Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256B M87C257	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz		
		– 168 hrs	672	0
		– 500 hrs	624	0
		– 1000 hrs	576	0
		– 2000 hrs	144	0
Retention Bake	1008	150°C,		
		– 168 hrs	817	0
		– 500 hrs	817	0
		– 1000 hrs	817	0
		– 2000 hrs	120	0

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 8. CMOS E5/0.8µm Process (–10% Upgrade) OTP ROM Reliability Data, Package Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256B M87C257	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,		
		– 168 hrs	500	0
		– 500 hrs	500	0
		– 1000 hrs	500	0
		– 2000 hrs	150	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,		
		– 48 hrs	504	0
		– 96 hrs	504	0
		– 168 hrs	448	0
		– 240 hrs	112	0
Pressure Pot		121°C, 2Atm,		
		– 48 hrs	1,260	0
		– 96 hrs	1,260	0
		– 168 hrs	1,260	0
		– 240 hrs	1,260	0
Temperature Cycling	1010	–40 to 150°C,		
		– 100 cycles	1,200	0
		– 500 cycles	1,200	0
		– 1000 cycles	1,000	0
Solderability:				
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	115	0
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	50	0
Resistance to Solvents	2015	4 Solvent Solutions	124	0

Table 9. CMOS E5/0.8µm Process (–20% Upgrade) OTP ROM Reliability Data, Die Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C512		M27C1001		M27C1024		M27C2001		M27C4001		M27C4002	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz												
		– 168 hrs	288	0	332	0	288	0	96	0	336	0	432	0
		– 500 hrs	240	0	284	0	240	0	96	0	336	0	432	0
		– 1000 hrs	192	0	236	0	192	0	96	0	336	0	336	0
		– 2000 hrs	48	0	44	0	48	0	-	-	96	0	48	0
Retention Bake	1008	150°C,												
		– 168 hrs	420	0	360	0	350	0	100	0	420	0	470	0
		– 500 hrs	420	0	360	0	350	0	100	0	420	0	470	0
		– 1000 hrs	420	0	300	0	290	0	100	0	420	0	470	0
		– 2000 hrs	60	0	60	0	120	0	-	-	120	0	60	0

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 10. CMOS E5/0.8µm Process (–20% Upgrade) OTP ROM Reliability Data, Package Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C512		M27C1001		M27C1024		M27C2001		M27C4001		M27C4002	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,												
		– 168 hrs	350	0	249	0	350	0	96	0	350	0	350	0
		– 500 hrs	350	0	249	0	350	0	96	0	350	0	350	0
		– 1000 hrs	350	0	249	0	350	0	96	0	350	0	300	0
		– 2000 hrs	100	0	50	0	100	0	-	-	50	0	50	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,												
		– 48 hrs	140	0	167	0	224	0	48	0	195	0	224	0
		– 96 hrs	140	0	167	0	224	0	48	0	195	0	224	0
		– 168 hrs	140	0	112	0	168	0	48	-	195	0	196	0
		– 240 hrs	112	0	28	0	56	0	48	-	55	0	28	0
Pressure Pot		121°C, 2Atm,												
		– 48 hrs	680	0	360	0	471	0	50	0	535	0	480	0
		– 96 hrs	680	0	360	0	471	0	50	0	535	0	480	0
		– 168 hrs	680	0	360	0	471	0	50	0	535	0	480	0
		– 240 hrs	480	0	300	0	471	0	50	0	535	0	480	0
Temperature Cycling	1010	–40 to 150°C,												
		– 100 cycles	480	0	360	0	360	0	40	0	360	0	420	0
		– 500 cycles	480	0	360	0	360	0	40	0	360	0	420	0
		– 1000 cycles	420	0	360	0	360	0	40	0	360	0	360	0
Solderability:														
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 502/0											
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 125/0											
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 328/0											

Table 11. CMOS E5/0.8µm Process (–35% Upgrade) OTP ROM Reliability Data, Die Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (E)		M27C2001 (E)		M27C4001 (E)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz						
		– 168 hrs	123	0	199	0	409	0
		– 500 hrs	123	0	199	0	409	0
		– 1000 hrs	123	0	199	0	313	0
		– 2000 hrs	-	-	-	-	-	-
Retention Bake	1008	150°C,						
		– 168 hrs	104	0	162	0	384	0
		– 500 hrs	104	0	162	0	384	0
		– 1000 hrs	104	0	162	0	384	0
		– 2000 hrs	-	-	-	-	-	-

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 12. CMOS E5/0.8µm Process (–35% Upgrade) OTP ROM Reliability Data, Package Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (E)		M27C2001 (E)		M27C4001 (E)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	105	0	160	0	310	0
		– 500 hrs	105	0	160	0	310	0
		– 1000 hrs	105	0	160	0	260	0
		– 2000 hrs	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	-	-	-	-	112	0
		– 96 hrs	-	-	-	-	112	0
		– 168 hrs	-	-	-	-	112	0
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	100	0	165	0	377	0
		– 96 hrs	100	0	165	0	377	0
		– 168 hrs	100	0	165	0	377	0
		– 240 hrs	100	0	165	0	377	0
Temperature Cycling	1010	–40 to 150°C,						
		– 100 cycles	105	0	160	0	519	0
		– 500 cycles	105	0	160	0	519	0
		– 1000 cycles	105	0	160	0	519	0
Solderability:								
– PLCC/TSOP Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 225/0					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 100/0					
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 80/0					

Table 13. CMOS T4/1.2µm Process FLASH MEMORY Reliability Data, Die Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 - M28F256A		M28F512	
			Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V, f = 500kHz,				
		– 24 hrs	48,256	0	112,488	0
		– 168 hrs	528	0	386	0
		– 500 hrs	528	0	386	0
		– 1000 hrs	480	0	338	0
		– 2000 hrs	96	0	96	0
Retention Bake (1)	1008	150°C,				
		– 168 hrs	547	0	1.042	0
		– 500 hrs	547	0	1,042	0
		– 1000 hrs	499	0	967	0
		– 2000 hrs	100	0	300	0
Write/Erase Cycling		1,000 cycles	4,122	1 (a)	15,831	2 (a)
		10,000 cycles	115	0	639	1 (b)
Retention Bake	1008	150°C, 36 hrs	4,122	0	15,831	0

Notes: 1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.
a. Programming Failure, single bit failures.
b. Erasing Failure, single bit failures.

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

– Electromigration in metal connections
– Contact spiking
– Process contamination
– Oxides defects
– Misplaced or weakened wire bonds
– Damaged wires
– Device surface damage

Table 14. CMOS T4/1.2µm Process FLASH MEMORY Reliability Data, Package Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 - M28F256A		M28F512	
			Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,				
		– 168 hrs	496	0	399	0
		– 500 hrs	496	0	399	0
		– 1000 hrs	496	0	349	0
		– 2000 hrs	100	0	149	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,				
		– 48 hrs	303	0	164	0
		– 96 hrs	303	0	164	0
		– 168 hrs	303	0	164	0
		– 240 hrs	137	0	83	0
Pressure Pot		121°C, 2Atm,				
		– 48 hrs	425	0	360	0
		– 96 hrs	425	0	360	0
		– 168 hrs	425	0	360	0
		– 240 hrs	345	0	360	0
Temperature Cycling	1010	–40 to 150°C,				
		– 100 cycles	300	0	270	0
		– 500 cycles	300	0	270	0
		– 1000 cycles	300	0	270	0
Thermal Shock	1011	–55 to 125°C,				
		– 100 cycles	-	-	30	0
		– 500 cycles	-	-	-	-
Solderability:						
– TSOP, PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 584/0			
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 80/0			
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 420/0			

Table 15. CMOS T5/0.8µm Process FLASH MEMORY Reliability Data, Die Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F101		M28F102	
			Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V, f = 500kHz,				
		– 24 hrs	139,816	0	17,761	0
		– 168 hrs	1,119	0	324	0
		– 500 hrs	1,071	0	324	0
		– 1000 hrs	973	0	276	0
		– 2000 hrs	135	0	48	0
Retention Bake (1)	1008	150°C,				
		– 168 hrs	894	0	100	0
		– 500 hrs	894	0	100	0
		– 1000 hrs	744	0	100	0
		– 2000 hrs	144	0	50	0
Retention Bake	1008	250°C,				
		– 168 hrs	869	0	-	-
		– 500 hrs	869	0	-	-
		– 1000 hrs	586	0	-	-
		– 2000 hrs	117	0	-	-
Write/Erase Cycling		1,000 cycles	26,201	3 (a)	3,010	0
		10,000 cycles	1,066	4 (b)	81	0
Retention Bake	1008	150°C, 36 hrs	26,201	0	3,010	0

Notes: 1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.
a. Programming Failure, single bit failure.
b. Erasing Failure, single bit failure.

Table 16. CMOS T5/0.8µm Process FLASH MEMORY Reliability Data, Package Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F101		M28F102	
			Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,				
		– 168 hrs	400	0	50	0
		– 500 hrs	400	0	50	0
		– 1000 hrs	350	0	50	0
		– 2000 hrs	-	-	50	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,				
		– 48 hrs	223	0	55	0
		– 96 hrs	223	0	55	0
		– 168 hrs	223	0	55	0
		– 240 hrs	28	0	55	0
Pressure Pot		121°C, 2Atm,				
		– 48 hrs	864	0	80	0
		– 96 hrs	864	0	80	0
		– 168 hrs	864	0	80	0
		– 240 hrs	843	0	80	0
Temperature Cycling	1010	–40 to 150°C,				
		– 100 cycles	870	0	60	0
		– 500 cycles	870	0	60	0
		– 1000 cycles	360	0	60	0
Thermal Shock	1011	–55 to 125°C,				
		– 100 cycles	50	0	-	-
		– 500 cycles	-	-	-	-
Solderability:						
– TSOP, PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 788/0			
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 425/0			
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 396/0			

Table 17. CMOS F3/1.5µm Process EEPROM Reliability Data, Die Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST93C06 ST93C46 ST93CS46A		ST93C56 ST93CS56		ST93C66 ST93CS66	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,						
		– 24 hrs	4,300	0	3,150	0	-	-
		– 168 hrs	300	0	150	0	-	-
		– 500 hrs	300	0	150	0	-	-
Retention Bake	1008	150°C,						
		– 500 hrs	150	0	100	0	50	0
		– 1000 hrs	100	0	-	-	-	0
Write/Erase Cycling		1,000,000 cycles	200	0	150	0	50	0
Retention Bake	1008	150°C, 168 hrs	200	0	150	0	50	0

Table 18. CMOS F3/1.5µm Process EEPROM Reliability Data, Package Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C04		ST93C06 ST93C46 ST93CS46A		ST93C66 ST93CS66	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	50	0	-	-	-	-
		– 500 hrs	50	0	-	-	-	-
		– 1000 hrs	50	0	-	-	-	-
Pressure Pot		121°C, 2Atm,						
		– 168 hrs	50	0	50	0	-	-
		– 240 hrs	50	0	50	0	-	-
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	50	0	50	0	-	-
Solderability:								
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = -/-					
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 100/0					
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 100/0					
Resistance to Surface Mount								
– SO Package			Cumulative Sample/Fail = 850/0					

Table 19A. CMOS F4/1.2µm Process EEPROM Reliability Data, Die Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01C ST24W01C		ST24C02C ST24W02C		ST24C04C ST24W04C		ST24C08C		ST24C16C ST24W16 ST24E16D ST24164	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,										
		– 24 hrs	4,250	0	6,850	0	4,500	0	2,150	0	3,452	0
		– 168 hrs	250	0	850	0	500	0	150	0	452	0
		– 500 hrs	250	0	850	0	500	0	150	0	452	0
		– 1000 hrs	-	-	228	0	-	-	-	-	152	0
Retention Bake	1008	150°C,										
		– 168 hrs	100	0	880	0	150	0	100	0	319	0
		– 500 hrs	100	0	880	0	150	0	100	0	319	0
		– 1000 hrs	-	-	880	0	-	-	-	-	119	0
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-
Write/Erase Cycling		50,000 cycles	200	0	1,200	0	500	0	100	0	350	0
		100,000 cycles	200	0	1,200	0	500	0	100	0	350	0
		1,000,000 cycles	200	0	1,200	0	500	0	100	0	350	0
Retention Bake	1008	150°C, 168 hrs	200	0	1,200	0	500	0	100	0	350	0

Table 19B. CMOS F4/1.2µm Process EEPROM Reliability Data, Die Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28C64C		ST93C66C		ST93C06C ST93C46C		ST95P04C	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,								
		– 24 hrs	239	0	80	0	4,444	0	74	0
		– 168 hrs	239	0	80	0	2,444	0	74	0
		– 500 hrs	239	0	80	0	2,444	0	74	0
		– 1000 hrs	239	0	80	0	194	0	74	0
Retention Bake	1008	150°C,								
		– 168 hrs	765	0	60	0	740	0	120	0
		– 500 hrs	765	0	60	0	740	0	120	0
		– 1000 hrs	765	0	60	0	740	0	120	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Write/Erase Cycling		50,000 cycles	600	0	70	0	959	0	49	0
		100,000 cycles	600	1 (a)	70	0	959	0	49	0
		1,000,000 cycles	-	-	70	0	959	0	49	0
Retention Bake	1008	150°C, 168 hrs	600	0	70	0	959	0	49	0

Note: a. Failure analysis in progress.

Table 20. CMOS F4/1.2µm Process EEPROM Reliability Data, Package Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01C ST24W01C		ST24C02C ST24W02C		ST24C04C ST24W04C		ST24C08C		ST24C16C ST24W16 ST24E16D ST24164		M28C64C		ST93C06C ST93C46C	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,														
		– 168 hrs	-	-	780	0	60	0	100	0	90	0	406	0	1,330	0
		– 500 hrs	-	-	780	0	60	0	100	0	90	0	406	0	1,330	0
		– 1000 hrs	-	-	780	0	60	0	100	0	90	0	406	0	1,330	0
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,														
		– 48 hrs	200	0	1,279	0	450	0	100	0	300	0	1,825	0	750	0
		– 96 hrs	200	0	1,279	0	450	0	100	0	300	0	1,825	0	750	0
		– 168 hrs	200	0	1,279	0	450	0	100	0	300	0	1,825	0	750	0
		– 240 hrs	200	0	1,279	0	450	0	100	0	300	0	1,825	0	750	0
Temperature Cycling	1010	–65 to 150°C,														
		– 100 cycles	200	0	1,650	0	450	0	100	0	300	0	1,908	0	700	0
		– 200 cycles	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		–40 to 150°C,														
		– 500 cycles	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Solderability:																
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 912/0													
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 496/0													
– PLCC Package			Cumulative Sample/Fail = 75/0													
– TSOP Package			Cumulative Sample/Fail = 239/0													
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 592/0													
Resististance to Surface Mount:																
– SO Package			Cumulative Sample/Fail = 1,000/0													
– TSOP Package			Cumulative Sample/Fail = 162/0													

Table 21. CMOS SPECTRUM/2.0µm Process ZEROPOWER SRAM Reliability Data, Die Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48Z02		MK48T02	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f =1MHz				
		– 168 hrs	154	0	288	0
		– 500 hrs	154	0	288	0
		– 1000 hrs	154	0	288	0

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 22. CMOS SPECTRUM/2.0μm Process ZEROPOWER SRAM Reliability Data, Package Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48Z02		MK48T02	
			Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 231 231 231	 0 0 0	 308 308 308	 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 300 cycles	 231 231	 0 0	 288 288	 0 0
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 96/0			

Table 23. HCMOS S3/1.2μm Process ZEROPOWER SRAM and FIFO Reliability Data, Die Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T08		MK48Z08		MK45H01	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f =1KHz						
		– 168 hrs	308	0	301	0	77	0
		– 500 hrs	308	0	301	0	77	0
		– 1000 hrs	308	0	301	0	77	0

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 24. HCMOS S3/1.2µm Process ZEROPOWER SRAM and FIFO Reliability Data, Package Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T08		MK48Z08		MK45H01	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 281 281 281	 0 0 0	 231 231 231	 0 0 0	 77 77 77	 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 300 cycles	 251 251	 0 0	 134 134	 0 0	 77 77	 0 0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 168 hrs	 - -	 - -	 - -	 - -	 89 89	 0 0
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 140/0					

Table 25. HCMOS 4P/0.7μm Process SRAM Reliability Data, Die Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M628128		MK62486		M628032	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f =1MHz						
		– 168 hrs	514	2 (a)	411	0	700	0
		– 500 hrs	512	1 (a)	411	0	700	0
		– 1000 hrs	435	1 (a)	411	0	700	0

Note: a. Single bit masking defect caused by polysilicon particle. Multiple process improvements have been implemented to address polysilicon particle reduction, and have been verified to reduce defects.

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 26. HCMOS 4P/0.7µm Process SRAM Reliability Data, Package Related Tests, April 1994 to March 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M628128		MK62486		M628032	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 154 154 154	 0 0 0	 231 231 230	 0 1 (a) 0	 77 77 77	 0 0 0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 192 hrs	 44 -	 0 -	 89 -	 0 -	 22 -	 0 -
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 300 cycles	 291 291	 0 0	 154 154	 0 0	 77 76	 1 (a) 2 (a)
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 128/0					

Notes: a. Single bit masking defect caused by polysilicon particle. Multiple process improvements have been implemented to address polysilicon particle reduction, and have been verified to reduce defects.

STATISTICAL PROCESS CONTROL

NMOS E3/1.5µm Process UV EPROM, Rousset - France Diffusion Line

Key Process Parameters	2Q 94		3Q 94		4Q 94		1Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Gate Oxide Thickness	1.42	1.34	1.38	1.32	1.34	1.29	1.25	1.04
Interpoly Oxide Thickness	1.45	1.44	1.21	1.11	2.05	1.11	1.53	1.45
Field Oxide Thickness	2.78	2.77	2.03	1.94	1.78	1.59	1.68	1.52
Intermediate Dielectric Thickness	4.40	4.17	3.64	3.57	4.52	4.40	7.28	7.02
Final P-Vapox Thickness	1.48	1.43	1.67	1.61	6.06	4.90	3.99	3.76
Polysilicon I Thickness	2.28	2.23	1.41	1.37	2.82	2.77	1.43	1.39
Polysilicon II Thickness	2.46	2.36	2.07	2.01	2.47	2.36	1.89	1.82
Aluminium 1% Si Thickness (SP1)	2.27	2.15	2.21	2.11	2.31	2.18	2.09	1.97
Polysilicon II Critical Dimensions	1.67	1.65	2.21	1.86	1.88	1.55	2.20	1.80
Active Area Critical Dimensions	2.41	2.04	1.65	1.61	3.67	3.13	1.44	1.36

Key Electrical Parameters	2Q 94		3Q 94		4Q 94		1Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT Henancement 25 x 25 µm	3.04	3.00	2.92	2.85	2.17	2.13	2.98	2.78
VT Array 25 x 25 µm	2.52	2.41	4.03	3.81	2.85	2.45	4.50	4.06
VT Field	5.52	2.72	6.10	2.86	7.83	3.77	11.80	5.12
I_{DON} Depletion 25 x 25 µm (1)	2.52	2.01	0.97	0.96	2.35	2.12	2.94	2.71
Polysilicon II Sheet Resistance	12.08	3.51	11.60	3.22	13.30	3.58	13.30	3.47
Buried Contact Chain Resistance	9.27	1.82	28.70	5.51	25.10	4.88	36.60	6.85
N+ Sheet Resistance	6.65	5.70	9.68	8.08	7.77	6.39	3.07	2.59
AL-Polysilicon II Contact Chain Resistance	12.90	5.64	9.31	4.02	9.91	4.55	12.80	5.74
AL-N+ Contact Chain Resistance	10.80	8.52	8.45	6.52	6.52	5.29	7.64	6.26

Note: 1. Probe card problem at electrical test before EWS.

Big oscillation quarter to quarter of CP/CPK on resistances are due to test problems and the difficulty to screen these wrong values.

STATISTICAL PROCESS CONTROL

CMOS E5/0.8µm Process UV EPROM and OTP ROM, Agrate - Italy R1 Diffusion Line

Key Process Parameters	2Q 94		3Q 94		4Q 94		1Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Pad Oxide Thickness	2.22	2.20	2.20	2.27	2.26	2.20	2.23	2.22
Silicon Nitride Thickness	1.84	1.80	1.54	1.52	2.00	1.96	2.01	1.99
Field Oxide Thickness	1.36	1.34	1.51	1.41	1.37	1.34	1.41	1.40
Gate Oxide Thickness	1.95	1.91	2.32	2.31	2.02	1.89	2.01	1.95
Interpoly Oxide Thickness	1.57	1.33	1.60	1.59	1.59	1.57	1.90	1.82
Intermediate Dielectric Thickness	1.48	1.43	2.48	2.35	1.79	1.76	2.08	2.02
Polysilicon I Thickness	1.47	1.41	1.41	1.36	1.65	1.60	1.72	1.64
Active Area Critical Dimensions	1.85	1.80	2.75	2.32	1.97	1.74	1.94	1.69
Policide Critical Dimensions	1.92	1.64	2.45	2.26	1.80	1.62	1.53	1.41

Key Electrical Parameters	2Q 94		3Q 94		4Q 94		1Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 µm	3.15	2.56	3.23	2.71	4.66	4.03	2.55	2.19
VT P-Channel 25 x 25 µm	1.64	1.52	2.27	2.00	2.04	1.86	2.58	2.14
VT Natural 25 x 25 µm	4.09	3.64	4.57	4.16	3.92	3.54	4.25	3.91
VT Memory Cell 0.8 x 0.8 µm	1.78	1.74	1.91	1.86	1.97	1.63	1.66	1.64
I_{DON} N-Channel 25 x 0.8 µm	1.90	1.46	3.40	2.84	3.23	3.05	3.10	2.98
N+ Active Area Contact Chain	3.55	1.55	4.42	3.36	3.82	3.35	5.73	4.46
AL-Tungsten Silicide Contact Chain Resistance	4.69	3.02	4.36	2.85	2.87	2.49	2.04	1.77

STATISTICAL PROCESS CONTROL

CMOS E5/0.8µm Process UV EPROM and OTP ROM, Agrate - Italy F8 Diffusion Line

Key Process Parameters	2Q 94		3Q 94		4Q 94		1Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Pad Oxide Thickness	1.71	1.70	1.77	1.76	1.73	1.70	1.65	1.56
Silicon Nitride Thickness	2.08	2.06	1.96	1.94	1.57	1.40	1.50	1.34
Field Oxide Thickness	2.36	2.33	2.02	1.96	2.03	2.00	1.65	1.65
Gate Oxide Thickness	1.53	1.49	1.68	1.64	1.48	1.48	1.35	1.29
Interpoly Oxide Thickness	1.43	1.41	1.42	1.34	1.38	1.36	1.61	1.51
Intermediate Dielectric Thickness	1.71	1.68	1.71	1.69	1.81	1.59	1.85	1.81
Polysilicon I Thickness	2.79	2.70	2.60	2.57	2.98	2.96	2.80	2.74
Active Area Critical Dimensions	1.90	1.75	1.85	1.83	2.29	2.28	2.10	2.00
Policide Critical Dimensions	1.32	1.20	1.33	1.32	1.63	1.45	1.70	1.70

Key Electrical Parameters	2Q 94		3Q 94		4Q 94		1Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 µm	2.31	2.19	2.21	2.21	2.09	1.60	2.06	1.52
VT P-Channel 25 x 25 µm	2.14	2.02	2.06	1.84	2.20	1.77	2.70	2.24
VT Natural 25 x 25 µm	2.93	2.84	3.10	2.07	3.14	2.69	2.15	1.99
VT Memory Cell 0.8 x 0.8 µm	1.30	1.28	1.25	1.23	1.27	1.21	1.32	1.15
I_{DON} N-Channel 25 x 0.8 µm	3.05	3.25	2.71	2.53	1.84	1.73	2.02	1.94
N+ Active Area Contact Chain	2.88	1.38	4.10	2.54	4.51	3.87	6.04	5.29
AL-W Silicide Contact Chain Resistance	1.21	1.21	1.43	1.21	4.26	2.40	1.37	1.32

STATISTICAL PROCESS CONTROL

CMOS T4/1.2μm Process FLASH MEMORY, Agrate - Italy R1 Diffusion Line

Key Process Parameters	2Q 94		3Q 94		4Q 94		1Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Field Oxide Thickness	1.36	1.34	1.51	1.50	1.37	1.35	1.41	1.40
Polysilicon I Thickness	1.47	1.41	1.41	1.36	1.65	1.60	1.72	1.64
Gate Oxide Thickness	2.25	2.23	2.30	2.25	2.10	2.10	2.12	2.06
Tunnel Oxide Thickness	1.46	1.45	1.47	1.44	1.42	1.39	1.43	1.41
ONO Bottom Oxide Thickness	2.07	2.05	1.32	1.29	1.74	1.40	1.58	1.57
ONO Nitride Thickness	1.35	1.32	1.24	1.20	1.34	1.30	1.26	1.25
ONO Top Oxide Thickness	1.04	1.03	2.10	2.10	2.21	2.19	1.96	1.93
Active Area Critical Dimensions	2.36	1.98	1.45	1.43	1.97	1.45	1.56	1.54
Polysilicon II Critical Dimensions	2.38	2.35	1.43	1.37	1.80	1.60	1.54	1.52

1Key Electrical Parameters	2Q 94		3Q 94		4Q 94		1Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 μm	2.79	2.39	3.64	3.00	2.67	2.09	2.24	2.22
VT P-Channel 25 x 25 μm	1.95	1.92	1.74	1.72	1.74	1.43	1.92	1.85
BV N-Channel 25 x 1.2 μm	1.52	1.33	1.56	1.43	1.45	1.41	1.44	1.41
BV P-Channel 25 x 1.6 μm	7.01	5.71	6.78	4.51	4.34	3.95	3.97	3.95
VT Memory Cell 0.8 x 0.8 μm	2.38	1.89	1.78	1.41	1.39	1.37	1.20	1.18
I_{DON} N-Channel 25 x 1.2 μm	1.99	1.90	1.80	1.67	2.04	1.34	1.78	1.78
Al-N+ Contact Chain	1.65	1.39	1.47	1.25	1.51	1.36	1.35	1.34
AL-W Silicide Contact Chain Resistance	1.86	1.71	1.54	1.48	1.53	1.45	1.45	1.43

STATISTICAL PROCESS CONTROL

CMOS T5/0.8µm Process FLASH MEMORY, Agrate - Italy R1 Diffusion Line

Key Process Parameters	2Q 94		3Q 94		4Q 94		1Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Field Oxide Thickness	1.36	1.34	1.51	1.50	1.37	1.35	1.41	1.40
Polysilicon I Thickness	1.47	1.41	1.41	1.36	1.65	1.60	1.72	1.64
Gate Oxide Thickness	2.25	2.23	2.30	2.25	2.10	2.10	2.12	2.06
Tunnel Oxide Thickness	1.46	1.45	1.47	1.44	1.42	1.39	1.43	1.41
ONO Bottom Oxide Thickness	2.07	2.05	1.32	1.29	1.74	1.40	1.58	1.57
ONO Nitride Thickness	1.35	1.32	1.24	1.20	1.34	1.30	1.26	1.25
ONO Top Oxide Thickness	1.04	1.03	2.10	2.10	2.21	2.19	1.96	1.93
Active Area Critical Dimensions	1.98	1.84	1.46	1.38	1.83	1.40	1.44	1.42
Polysilicon II Critical Dimensions	1.74	1.74	2.09	1.92	1.62	1.39	1.18 (1)	0.87

Key Electrical Parameters	2Q 94		3Q 94		4Q 94		1Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 µm	2.46	1.82	2.64	2.11	2.38	1.81	2.80	2.79
VT P-Channel 25 x 25 µm	2.07	1.86	2.38	2.13	2.27	2.01	1.89	1.77
BV N-Channel 25 x 0.8 µm	3.93	3.60	4.94	4.33	4.54	3.90	4.59	4.59
BV P-Channel 25 x 0.9 µm	2.19	2.09	3.01	2.44	2.86	2.61	5.70	5.64
VT Memory Cell 0.8 x 0.8 µm (1)	1.44	1.36	2.80	2.23	1.88	1.71	2.10	2.04
I_{DON} N-Channel 25 x 1.2 µm	2.18	1.53	3.00	2.55	2.24	1.84	2.24	2.14
Al-N+ Contact Chain	2.73	2.36	4.49	4.18	4.59	4.15	2.89	2.80
Al-W Silicide Contact Chain Resistance	2.05	1.97	1.80	1.59	2.56	2.50	2.62	2.60

Note: 1. Low CPK is due to change of dimensional target to improve the access time.

STATISTICAL PROCESS CONTROL

UV EPROM Assembly Line, Singapore, Ceramic Frit-Seal Package

Key Process Parameters	2Q 94		3Q 94		4Q 94		1Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Shear Test (D.A.)	(*)	2.67	(*)	3.69	(*)	5.00	(*)	3.66
Bond Strength (W.B.)	(*)	2.57	(*)	2.63	(*)	2.77	(*)	2.59
SN Thickness (Tin Plate)	1.73	1.34	1.75	1.63	1.70	1.85	1.62	1.43
Lead Lenght (Cropping)	2.65	2.14	2.55	1.55	2.00	2.80	1.78	2.66

Note: *. One side limit only (CPL).

FAILURE RATE PREDICTIONS

April 1994 to March 1995

Process	Actual Device hrs		Temperature Activation Energy (eV)	Voltage Acceleration Factor	Equivalent hrs 55 °C (x 10^6)	Life Test Failure	Failure Rate (Fit) Confidence Level	
	Dev. hrs (x 10^6)	Temp. (°C)					60%	90%
UV EPROM								
CMOS E5 -20%	6.08	140	0.6	4.0	1,670	1	1.2	2.3
CMOS E5 -35%	3.70	140	0.6	4.0	1,017	0	0.9	2.2
NMOS E3	5.14	140	0.6	2.6	666	0	1.4	3.5
OTP								
CMOS E5 -20%	1.81	140	0.6	4.0	470	0	1.9	4.9
CMOS E5 -35%	0.68	140	0.6	4.0	177	0	5.2	13.0
FLASH								
CMOS T4	4.89	140	0.6	3.0	951	0	0.9	2.4
CMOS T5	5.26	140	0.6	4.0	1,363	0	0.7	1.7
SRAM								
CMOS Spectrum	0.44	125	0.7	4.0	136	0	6.7	17.0
HCMOS S3	0.68	125	0.7	4.0	211	0	4.3	11.0
HCMOS S4P	1.58	125	0.7	5.7	697	4	7.5	11.0
EEPROM								
CMOS F4	3.40	140	0.6	3.0	800	0	1.1	2.9